**Hardik J Patel           EEC 180A**

**Lab 3 Report – Combinational Network Design using Muxes and Adders**

**July 9, 2015**

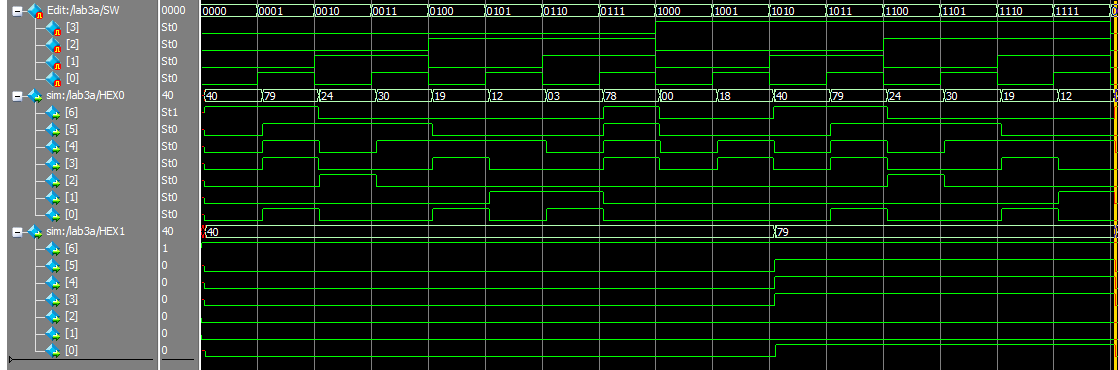
**Objective**

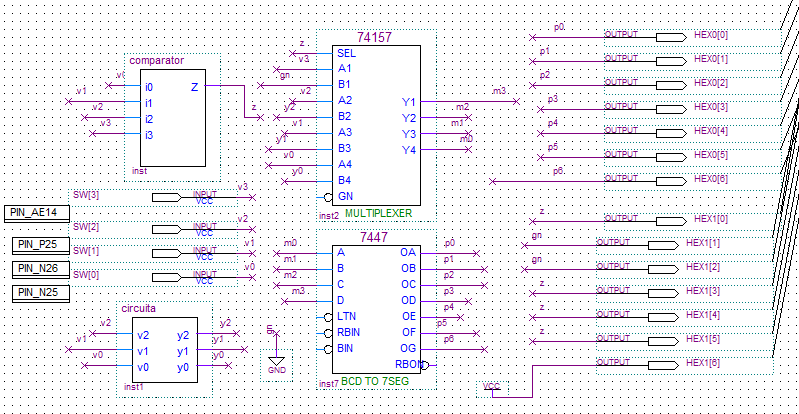
The purpose of this lab was to learn designing circuits using multiplexers and adders, to create symbols for different components used in the lab to make the project easier to understand and follow. One of the objectives of part 2 of this lab was to measure and understand the maximum propagation delay of the ripple-carry adder. The designs were simulated on ModelSim-Altera to analyze the different input and output waveforms and verified on the DE2 board to ensure accurate working of the designs.

**Design and Test Procedure**

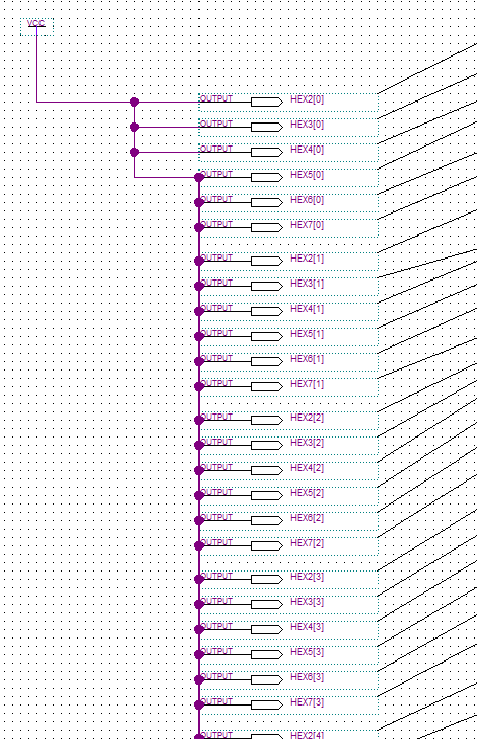
Part 1: The problem for this lab instructed us to convert a four bit binary number to its equivalent decimal form. For this purpose the prelab instructed us to generate truth tables for different components used to design this circuit. Once the truth tables were generated the design for the comparator and circuit A were built on different files in the project (this was done to simplify the design of the top level entity). Once the two designs were completed, symbols for both were generated and included in the main file and the design was completed. The design was run, simulated in ModelSim-Altera and verified on the DE2 Board.

**ModelSim-Altera simulation of part 1 design:**



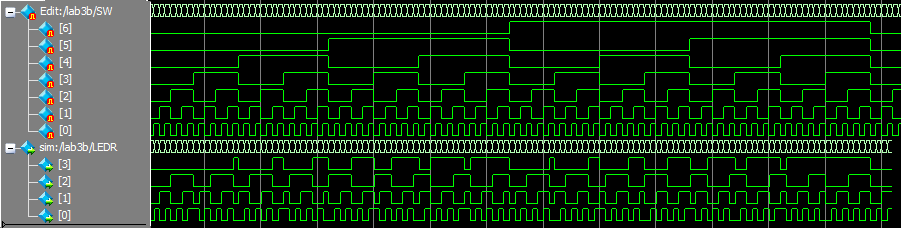
**Schematic of part 1 design:**

The comparator and circuit A components as seen above are the symbols for their respective designs.

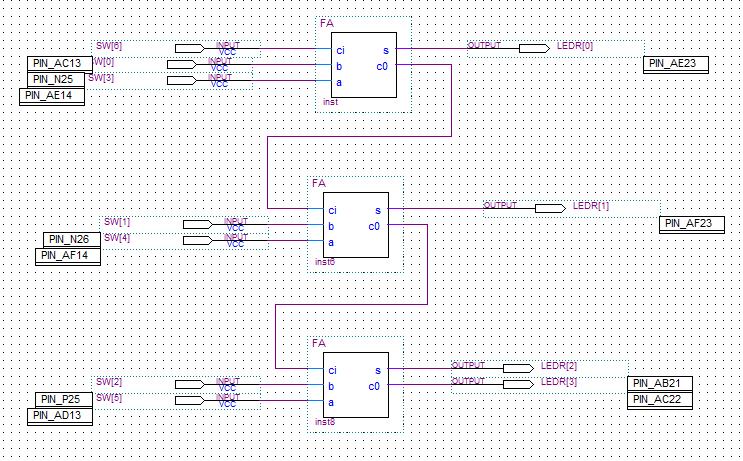


Part 2: This part of the lab included designing a Full Adder, creating a symbol for the Adder and using it to design a Three-bit Ripple-Carry Adder. A full adder was first designed using the figure included in the lab and then a Ripple-Carry Adder was implemented. The design was run, simulated in ModelSim-Altera and verified on the DE2 Board.

**ModelSim-Altera Simulation of part 2 design:**

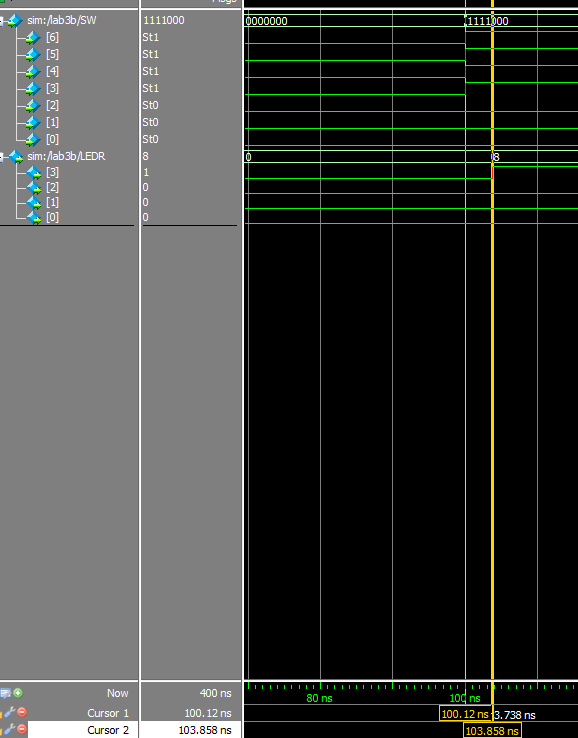
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**Schematic of part 2 design:**

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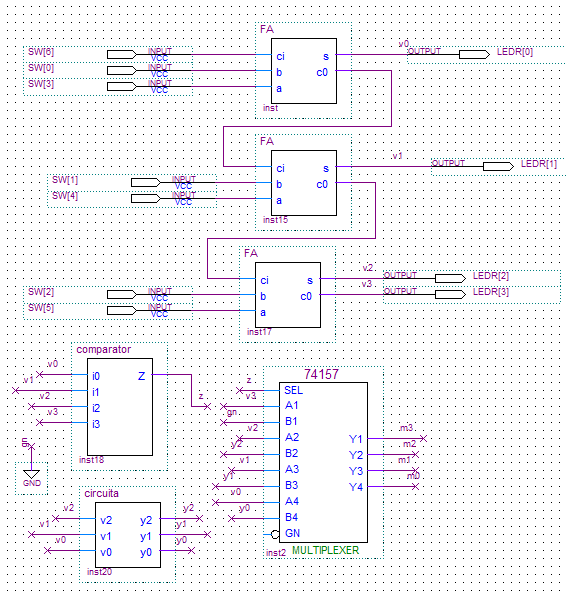
This design adds 2 three-bit numbers with the possibility of adding a carry in. Hence the maximum addition is 7+7+1=15. The sum of the two numbers is displayed on the LED segment of the DE2 board.

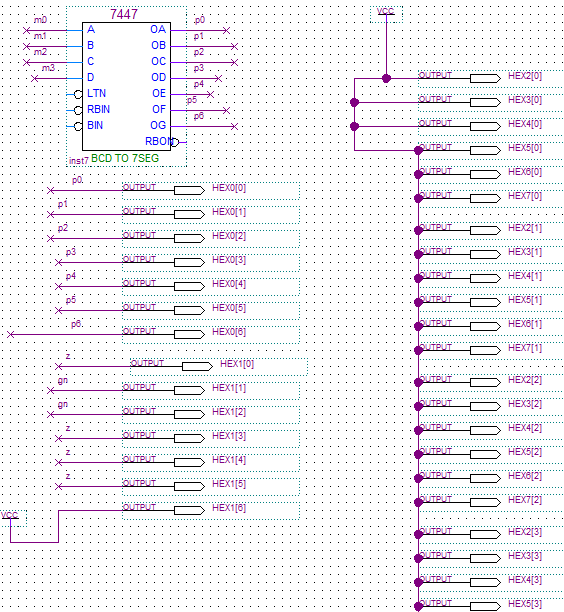
**ModelSim-Alter simulation to show maximum propagation delay:**



Part 3: For this part of the lab the two previous designs were combined to give one circuit. This was done by using the 4 outputs of part 2 as the inputs, v3…v0, of part 1. Hence the combined circuit becomes a three-bit ripple-carry adder with the output displayed in decimal and binary (on the LED strip).

**Schematic of part 3 design:**

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**Results**

The waveforms for each part are attached above. The truth table for the full adder is attached at the end.

Q. What is the ‘octal’ radix and why is it convenient to represent the SW[] input in octal in the Part II simulation? Why isn’t octal convenient for the LEDR[] output?

Ans. The SW[] inputs include three numbers, two of them use 3 inputs and the carry-in uses 1 input. Since the numbers are only three bit, the can count only from 0 upto 7, which is 8 digits. Hence it is convenient to use octal as it too has digits 0 to 7. For a similar reason LEDR[] output is represented in hexadecimal, since it has 4 digits and count from 0 to 15.

Q. Give the maximum propagation delay that you measured for your ripple-carry adder in ModelSim.

Ans. The maximum propagation delay as measured by the simulation came out to be 3.738 ns.

This experiment shows the practical working of binary to decimal converters as these are used everywhere. Also it shows the working and functionality of a full adder.

**Conclusion**

In this lab we learnt to crate symbols for certain subparts of a project to make the main file in the project easier to follow. Also the concepts of gate delay and maximum propagation delay for the ripple-carry adder were show in the ModelSim simulations.